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PROCESS PERTURBATION TO MEASURED-MODELED METHOD FOR SEMICONDUCTOR DEVICE TECHNOLOGY MODELING

Cross-Reference to Related Applications

[0001] This application is a continuation of and claims priority of U.S. Patent Application No. 60/200,302 filed on April 28, 2000.

[0002] This application is related to the following commonly-owned co-pending patent application, Serial No. 09/680, 339, filed on October 5, 2000: METHOD FOR UNIQUE DETERMINATION OF FET EQUIVALENT CIRCUIT MODE PARAMETERS, by Roger Tsai. This application is also related to the following commonly-owned co-pending patent applications all filed on April 28, 2000, S-PARAMETER MICROSCOPY FOR SEMICONDUCTOR DEVICES, by Roger Tsai, Serial No. 60/200,307, Docket No. 12-1114);EMBEDDING PARASITIC MODEL FOR Pi-FET LAYOUTS, by Roger Tsai, Serial No. 60/200,810, (Attorney Docket No. 12-1116; SEMI-PHYSICAL MODELING OF HEMT DC-TO-HIGH FREQUENCY ELECTROTHERMAL CHARACTERISTICS, by Roger Tsai, Serial No. 60/200/648, (Attorney Docket No. 12-1118; SEMI-PHYSICAL MODELING OF HEMT HIGH FREQUENCY NOISE EQUIVALENT CIRCUIT MODELS, by Roger Tsai, Serial No. 60/200,290, (Attorney Docket No. 12-1119); SEMI-PHYSICAL MODELING OF HEMT HIGH FREQUENCY SMALL SIGNAL EQUIVALENT CIRCUIT MODELS, by Roger Tsai, Serial No. 60/200,666, (Attorney Docket No. 12-1120); and HYBRID SEMI-PHYSICAL AND DATA FITTING HEMT MODELING APPROACH FOR

LARGE SIGNAL AND NON-LINEAR MICROWAVE/MILLIMETER WAVE CIRCUIT CAD, by Roger Tsai and Yaochung Chen, Serial No. 60/200,622, (Attorney Docket No. 12-1127.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0003] The present invention relates to a method for modeling semiconductor devices and more particularly to a method for modeling based upon a process perturbation to measured-to- modeled experimentation method for modeling semiconductor devices.

2. Description of the Prior Art

[0004] The capability to accurately forecast product yield of semiconductor devices, such as microwave monolithic integrated circuits (MMIC), is an invaluable asset in manufacturing. Yield forecasting allows for better allocation of limited manufacturing resources; identification of yield problems; and reduced manufacturing costs. In GaAs MMIC manufacturing, the drive to new markets under reduced design costs and reduced time-to-market cycles have increased the probability for RF yield problems. These risks become even more acute when RF performance specifications are pushed to the limits of the process in accordance with the current trend in an ever more competitive environment.

[0005] Addressing the cause of poor MMIC yield can be an insidious problem in that it may not be specific. In particular, RF yield problems may occur as a result of unrealized shortcomings distributed across the entire manufacturing process. The principle mechanisms which contribute to yield loss in an MMIC manufacturing process are illustrated in FIG. 1. As shown, four out of seven possible mechanisms relate strongly to RF yield loss. Factors, such as unrealistic performance specification; poor design-for-manufacturing; and process variability may individually or cumulatively reduce the RF yield, thus raising the long term manufacturing costs as well as the design to manufacturing cycle time.

[0006] Various methods are used for RF yield forecasting. For example, both statistical and empirical modeling methods are known. Statistical modeling employs device models and circuit simulation while empirical modeling uses measured data. Such statistical models include Monte Carlo statistical models, correlated statistical models, boundary models and database models. Monte Carlo statistical models allow device model parameters to vary independently of each other by Gausian statistics while correlated statistical models are known to represent more realistic statistics in which the variations are constrained with correlation between the model parameters. Long-term model databases are typically created for the purpose of process control monitoring but can also be used in yield forecasting, for example, as disclosed in "A Product Engineering Exercise in 6-Sigma Manufacturability: Redesign of pHEMT Wideband LNA, by M. King et al., 1999 GaAs MANTECH Technical Digest, pp. 91-94, April 1999.

[0007] Boundary models are a set of models that represent the "process corner performance". Boundary models are known to be ideal for quickly evaluating the robustness of a new design to an anticipated process variation. Some manufacturers are known to develop methods that directly evaluate robustness through "process corner experimentation", for example as disclosed "GaAs Fabs Approach to Design-for-Manufacturability", by R. Garcia, et al. 1999 GaAs MANTECH Technical Digest, pp. 99-102, April 1999. However, the boundary methods cannot be used to determine RF performance distributions that are fundamental to yield calculation. As such, this method is unsuitable for RF yield prediction.

[0008] Long-term model databases are a powerful tool for MMIC process control monitoring and typically consist of large samples of small signal equivalent circuit model extractions for single consistent device structures, measured under a standard set of bias conditions. Database models unambiguously capture true process variations through uniform sampling. Unfortunately, such models are limited to applications based closely around original measurements. For example, accurately extending a database model to represent a device with different bias conditions and layouts is problematic. Such determinations are labor intensive, as generally set forth in; "A Product Engineering Exercise in 6-Sigma Manufacturability: Redesign of a pHEMT

Wide-Band LNA," supra. In other circumstances, it is virtually impossible or unadvisable to apply database results, for example, to predict low noise or low signal results from a small signal model.

[0009] Monte Carlo statistics are simple to implement for RF yield simulations. However, forecasts produced by this method are relatively inaccurate and are normally used for worse case yield analysis. In particular, examples of inaccurate yield forecasts provided by Monte Carlo and correlated statistical models are shown in FIGS. 2A and 2B, which illustrate simulated versus actual noise and gain statistics for a 22-26 GHz GaAs pHEMT LNA. As illustrated, the squares and circles represent simulated data points by correlated statistical and Monte Carlo statistical models, respectively and the dashed line represents the measured data points.

[0010] Correlated statistical models provide a better method than the Monte Carlo method, however, the results from this method can also be inaccurate. Another drawback of correlated statistical models is that substantial model databases are also needed in order derive the correlation which subject method to restrictions that normally plague long-term model databases.

[0011] As mentioned above, empirical forecasting is also known to be used for forecasting RF yield. In such empirical forecasting methods, the long-term RF yield of one circuit is predicted by known process dependent RF yield characteristics of another circuit. This method can be thought of yield mapping which utilizes a linear mapping transformation between a critical RF performance parameter and the measured device process control monitor (PCM) data. This transform is known to be used to map PCM data into circuit performance space. Any distribution of PCM parameters are transformed into a distribution of RF performance. An example of such a transformation is shown in FIG. 3 which illustrates a transformation of a device PCM to MMIC RF performance space. To apply the yield map design to other circuits, an offset is included to account for differences associated with design. Such empirical methods are known to provide accurate forecasting of noise figure and small signal gain performance but not for power. An exemplary comparison of forecasted and measured noise figure performance for a 35 GHz GaAs pHEMT LNA is shown in FIG. 4 in which the forecasted data is shown with a line and measured data is shown by squares.

[0012] One drawback to yield mapping is that it cannot be used to accurately predict RF performance before the designs are produced. Instead its prediction must be refined as the design dependent offset becomes determined through feedback from the pre-production run.

[0013] Other empirical methods are known for forecasting RF yield parameter extraction using measured S-parameters. In such methods, the semiconductor device is modeled and parameters are extracted from the measured S-parameters using analytical techniques, for example, as disclosed in "A Semianalytical Parameter Extraction of a SPICE BSIM 3v3 for RF MOSFET's using S-Parameters", by Lee, et al., IEEE Transactions on Microwave Theory and Techniques, Vol. 48, No. 3, March 2000, pp. 4-416. Unfortunately, such a technique does not provide sufficiently accurate results to accurately forecast RF yield.

[0014] Unfortunately, to accurately model the characteristics of a semiconductor device, phenomenon associated with the internal structure of the device, such as, the length of the linear conductance region; the magnitude of saturating electrical fields; the effective transit distance for saturated carriers; and the like need to be considered. Finite element device simulations have been known to be used to calculate the internal electrical charge/electrical field structure of devices. Unfortunately, such device simulations are generally not accurate, thus providing results that can be significantly different from measured device electrical characteristics. As such, there is a lack of analytical techniques that can resolve and measure electrical properties associated with the internal structure of a semiconductor device to a method for accurately modeling semiconductor devices.

SUMMARY OF THE INVENTION

[0015] Briefly, the present invention relates to a method for modeling semiconductor devices which utilizes a measured-to-modeled microscope as a fundamental analysis basis for constructing a physically-based model by correlating measured-to-modeled performance changes to experimental device changes designed to controllably change physical aspects of the device. The effects of the process perturbation are attributed to changes in measurable internal characteristics of the

device. With thorough process perturbation to measured-modeled PM^2 experimentation, the full range of device performance can be expressed in terms of the microscope's model-basis space, thus forming a single unified compact device technology model, able to accurately model performance changes over a relatively wide range of possible physical and environment changes to the device. The device technology model is able to model internal physical operating mechanisms that dictate the electrical characteristics of the device, such as charge control in FET's or current control in BJT's.

DESCRIPTION OF THE DRAWINGS

[0016] These and other advantages of the present invention will be readily understood with reference to the following specification and attached drawings wherein:

[0017] FIG. 1 is a flow chart of MMIC yield loss mechanisms known in the manufacturing process.

[0018] FIG. 2A and 2B represent simulated versus cumulative yield for noise figure and gain, respectively, for a 26 GHz MMIC using Monte Carlo and correlated statistical device models, wherein the measured data is shown with squares; the Monte Carlo statistical data is shown with circles; and the measured data shown is with a dashed line. FIG. 3 is an exemplary representation illustrating a known mapping MMIC RF yield forecasting method.

[0019] FIG. 4 is a graphical illustration illustrating the measured noise factor versus the mapped noise factor for a 35 GHZ GaAs pHEMT LNA utilizing the method illustrated in FIG. 3.

[0020] FIG. 5 is a block diagram illustrating the semiconductor modeling in accordance with the present invention.

[0021] FIG. 6 is a block diagram of the present invention which relates to process perturbation to measured-model method for modeling semiconductors which utilizes S-parameter microscopy in accordance with the present invention.

[0022] FIG. 7A is a schematic cross-sectional diagram of a standard HEMT used in the PM^2 experiment.

[0023] FIG. 7B is a cross-sectional diagram illustrating the epistack for the exemplary HEMT device used to demonstrate the present invention.

[0024] FIG. 8 is schematic diagram illustrating the correspondence of the small signal equivalent circuit components to the detail of the device physical structure.

[0025] FIG. 9 is a schematic diagram of the source access conductance of the HEMT.

[0026] FIG. 10A is a graphical illustration of a source resistance R_s as a function of the biasing voltage V_{gs} for different drain-to-source voltages V_{ds}.

[0027] FIG. 10B is a graphical illustration of the source resistance R_s as a function of the gate-to-source voltage illustrating the measured vs. semi-physically modeled approaches.

[0028] FIG. 11 represents an exemplary S-parameter microscope in accordance with the present invention.

[0029] FIG 12 illustrates the internal and external regions of an exemplary HEMT device.

[0030] FIG. 13 is similar to FIG. 11 but illustrates the approximate locations of the model elements in the HEMT FET device illustrated is FIG. 11.

[0031] FIG. 14 is a schematic diagram of a common source FET equivalent circuit model.

[0032] FIG. 15 is an illustration of specific application of the S-parameter microscope illustrated in FIG. 11.

[0033] FIG. 16 is similar to FIG. 11 which demonstrates the inability of known systems to accurately predict the internal charge and electrical field structure of a semiconductor device.

[0034] FIG. 17 is a plan view of a four-fingered, 200μm GaAs HEMT device.

[0035] FIG. 18 is a graphical illustration illustrating the measured drain-to-source current I_{ds} as a function of drain-to-source voltage Vds for the sample FET device illustrated in FIG. 17.

[0036] FIG. 19 is a graphical illustration illustrating the drain-to-source current I_{ds} and transconductance G_m as a function of the gate-to-source voltage V_{gs} of the sample FET device illustrated in FIG. 17.

[0037] FIG. 20 is a Smith chart illustrating the measured S11, S12 and S22 parameters from frequencies of 0.05 to 40.0 GHZ for the FET device illustrated in FIG. 17.

[0038] FIG. 21 is a graphical illustration of the magnitude as a function of angle for the S21 S-parameter for frequencies of 0.05 to 40 GHz for the exemplary FET illustrated in FIG. 17.

[0039] FIG. 22 is a graphical illustration of a charge control map of the charge and electric field distribution in the on mesa source access region shown with R_s as a function bias in accordance with the present invention.

[0040] FIG. 23 is a graphical illustration of a charge control map of charge and electric field distribution in the on-mesa drain access region shown with R_d as a function of bias in accordance with the present invention.

[0041] FIG. 24 is a graphical illustration of a charge control map for the non-quasi static majority carrier transport, shown with R_i as a function of bias in accordance with the present invention.

[0042] FIG. 25 is a graphical illustration of a charge control map for gate modulated charge and distribution under the gate, shown with Cgs and Cgd as function of bias in accordance with the present invention.

[0043] FIG. 26 is a plan view of an exemplary π-FET with two gate fingers.

[0044] FIG. 27 is a plan view of a π-FET with four gate fingers.

[0045] FIG. 28 is an illustration of a π-FET parasitic model in accordance with the present invention.

[0046] FIG. 29 is an illustration of an off-mesa parasitic model for a π-FET in accordance with the present invention.

[0047] FIG. 30 is an illustration of an interconnect and boundary parasitic model in accordance with the present invention for the π-FET with four gate fingers as illustrated in FIG. 27.

[0048] FIG. 31 is an illustration of an inter-electrode parasitic model in accordance with the present invention.

[0049] FIG. 32 is a schematic diagram of the inter-electrode parasitic model illustrated in FIG. 31.

[0050] FIG. 33 is an illustration of an on-mesa parasitic model in accordance with the present invention.

[0051] FIG. 34 is a schematic diagram of the on-mesa parasitic model illustrated in FIG. 33.

[0052] FIG. 35 is an illustration of an intrinsic model in accordance with the present invention.

[0053] FIG. 36 is a schematic diagram of the intrinsic model illustrated in FIG. 35.

[0054] FIG. 37A is an exemplary device layout of a π-FET with four gate fingers.

[0055] FIG. 37B is an equivalent circuit model for the π-FET illustrated in FIG. 37A.

[0056] FIG. 38 is a single finger unit device cell intrinsic model in accordance with the present invention.

[0057] FIG. 39 is similar to FIG. 38 and illustrates the first level of embedding in accordance with the present invention.

[0058] FIG. 40 is similar to FIG. 38 and illustrates the second level of embedding in accordance with the present invention.

[0059] FIG. 41 is an equivalent circuit model of the π-FET illustrated in FIG. 37A in accordance with the present invention.

[0060] FIG. 42 is similar to FIG. 40 and illustrates the third level of embedding in accordance with the present invention.

[0061] FIG. 43 is similar to FIG. 40 and illustrates the fourth level of embedding in accordance with the present invention.

[0062] FIG. 44 is similar to FIG. 40 and illustrates the fifth level of embedding in accordance with the present invention.

[0063] FIG. 45A and 45B is a flow chart of a parameter extraction modeling algorithm that forms a part of the present invention.

[0064] FIGS. 46 and 47 represent an error metric in accordance with the present invention.

[0065] FIG 48A is a Smith chart illustrating the measured versus the initial model solutions for the S11, S12 and S22 S-parameters from frequencies from 0.05 to 40.0 GHz.

[0066] FIG. 48B is a graphical illustration of angle versus magnitude for the initially modeled S-parameter S21 from frequencies of 0.05 to 40 GHz.

[0067] FIG. 49A is a Smith chart illustrating the measured versus simulated S-parameters S11, S12 and S22 for frequencies 0.05 to 40 GHz for the first extraction optimization cycle.

[0068] FIG. 49B is a graphical illustration of magnitude as a function of angle for the measure and first optimized model S-21 parameter for frequencies 0.05 to 40 GHz for the first optimization cycle.

[0069] FIG. 50A is a Smith chart illustrating the measure as a function of the final model solution for S-parameters S11, S12 and S22 for frequencies 0.05 to 40 GHz for the final solution.

[0070] FIG. 50B is a graphical illustrations of the magnitude as a function of an angle for S-parameter S21 for the final model solution from frequency 0.05 to 40 GHz.

DETAILED DESCRIPTION

[0071] The present invention relates to a method for modeling semiconductor devices based upon a process perturbation to measured modeled (PM^2) methodology which can be used to develop a physically-based technology model that ultimately becomes more and more accurate as more and more process perturbation experiments are performed. As shown in FIG. 5, various parameters, such as device scaling, bias dependence, temperature dependence, layout dependence and process dependence can be modeled using this technique to analyze measurements taken for any imaginable set of process perturbations. The more measurements that are taken, physically-based technology model, or semi-physical model, becomes more and more "corrected". For example, by performing more PM^2 experiments in which the gate length of high electron mobility transistors (HEMT) samples are varied to much longer lengths than originally studied, the models for velocity saturation and effective gate source charge control length can be refined to provide more accurate results for longer gate lengths.

Also, by performing temperature dependent measurements the temperature dependence on the material parameters is able to be refined to better fit the modeled to the measured results.

[0072] An important part of the PM^2 modeling methodology is a measured-to-model microscope which is able to look into the "guts" of a semiconductor device. With this capability a relatively comprehensive physically-based model for the entire device technology can be developed.

[0073] The modeling approach in accordance with the invention is discussed below in connection with FIGS. 5-10. An important aspect of the invention is a measured-to-model microscope (i.e. S-parameter microscope), such as discussed below in connection with FIGS. 11-30. The measured-to-model microscope may utilize a filter in order to remove the contribution of device layout parasitics to the modeled electrical characteristics. This may be done to accomplish, clearer representations of the internal physical operation for the measured devices. One embodiment of such a filter for Pi-FET-type layouts is discussed in connection with FIGS. 26-44. The exemplary measured-to-model microscope utilizes an extraction algorithm for extracting modeled parameters as generally discussed in connection with FIGS. 45-50.

PROCESS PERTURBATION TO MEASURED-TO-MODELED METHOD FOR SEMICONDUCTOR DEVICE TECHNOLOGY MODELING

[0074] The following example illustrates the use of the PM^2 modeling concept to create a complete, physically-based model for the source resistance of a HEMT device. The PM^2 experiment used to determine the physical model characteristics are as follows:

[0075] 1) Characterize standard HEMT samples

[0076] A) Use standard fabrication processes to produce sample HEMT devices with a standard device layout.

[0077] B) Collect information regarding the physical dimensions of the source-access region by way of a scanning electron microscope (SEM).

[0078] C) Test the sample devices using S-parameter microscopy to establish physically representative equivalent electrical models.

[0079] 2) Characterize the standard HEMT samples with device layout experiments

[0080] A) Use standard fabrication processes to produce sample HEMT devices with device layout experiments that vary the physical dimensions of the source access region, for example, gate source spacing, etc.

[0081] B) Collect information regarding the physical dimensions of the source access region by way of a SEM.

[0082] C) Test the sample devices by way of S-parameter microscopy to establish physically representative equivalent electrical models.

[0083] 3) Characterize the HEMT samples with a thin GaAs "cap"

[0084] A) Use standard fabrication processes on the thin "cap" material to produce sample HEMT device with a standard device layout.

[0085] B) Collect information regarding the physical dimensions of the source access region by way of SEM.

[0086] C) Test the S-parameter microscopy to establish physically representative equivalent electrical models.

[0087] A cross-sectional diagram of the standard HEMT sample used in the example is illustrated in FIG. 7A. A diagram of a standard device layout for a Pi-FET example is shown in FIG. 37A. A cross-sectional diagram of the material epi-stack present in the standard HEMT is shown in FIG. 7B. For the third part of the PM^2 experiment above, the GaAs cap is thinned down to 7.5 nm instead of the standard thickness of 50 nm keeping the same doping density.

[0088] After sample wafers are fabricated for use as standard HEMT samples, Scanning Electron Microscopy (SEM) is used to determine the dimensions of the critical structural components. The measured and intended structural dimensions are identified in Table 1 below, where measured refers to SEM determined dimension and standard indicates the normal or intended specification. Each of the dimensions listed in Table 1 are correlated to the cross-sectional diagram illustrated in FIG. 7A.

Table 1
SEM Measured and Intended Structural Dimension for a "Standard"HEMT Device Sample

	units	Measured	Standard
Lg	[μm]	0.15	0.15
Dsg	[μm]	0.78	0.8
Dsd	[μm]	1.935	2
Lg+RECsg+RECgd	[μm]	0.56	0.52

[0089] Next, S-parameter microscopy as described below and in connection with FIGS. 11-25 and 45-50 is used to determine physically representative, model representations of the source access resistance. The exemplary Pi-FET may be modeled and used as a filter in the S-parameter microscopy as generally described in connection with FIGS. 26-44. S-parameter microscopy is accomplished by measuring the S-parameters of the sample devices up to 40 GHz and subsequently extracting equivalent small signal circuit models as discussed in detail below in connection with S-parameter microscopy. The small signal equivalent circuit model serves as an electrical representation of the physical structure of the measured device and can be used to roughly sketch the details of its internal structure. The correspondence between equivalent circuit elements and structural items within the device are shown in FIG. 8 below. The relationship of the quantity "Rs" and the source access region is shown.

[0090] The results of the S-parameter microscopy measurements are shown in FIG. 22 which plot the bias dependent characteristics of the source resistance Rs. From these bias dependent characteristics, a preliminary physical model which fits the measured data can be constructed.

[0091] Three physical effects were found to contribute to the overall behavior of the measured source resistance: resistance of the access region before the recess on the source side region; resistance within the source access recess; and a boundary resistance caused by sudden change in sheet carrier concentration between the source access region and the channel directly under the gate. These phenomena and their physical

locations within the source access recess are illustrated in FIG. 9 where regions 1, 2 and 3 correspond to each of the effects discussed above.

[0092] From these observations, a form of semi-physical model describing bias-dependent characteristics of Rs in a HEMT device can be established as set forth in the equations below.

$$R_S \quad [\Omega] \quad = (R_{SundepCap} + R_{SAccess} + R_{SBoundary}) / W_g$$

$$= R_{cont}/RF_{rconF} +$$

$$R_{S\,undepCap} \quad [\Omega*\mu m] \quad R_{SH}[D_{sg} - (REC_{sg}+L_g/2)]$$

[0093] In part two of the PM^2 experiment, the HEMT device samples are fabricated and tested and the length of the source access region is intentionally varied.

[0094] After the samples are fabricated, the intended dimensions are verified through SEM. S-parameter microscopy is also used to extract the source resistance for comparison. The experimental source gate dimensions along with the extracted source resistance are provided in Table 2 below.

Table 2

Extracted Source Resistance vs. Source-Gate Distance

	Dsg [μm]	Rs [Ω]
	0.4	1
	0.8	1.2
	1	1.3
	1.2	1.45
Measured Sheet Res:	109.1	Ω/sq
Extracted Sheet Res:	110	Ω/sq

[0095] The data in Table 2 is used to confirm the preliminary semi-physical model for Region 1's source-access resistance (Rsundep Cap) illustrated above. This confirmation can be verified by comparing the extracted sheet resistance (Rsh) by S-

parameter microscopy and the PM^2 experiments against sheet resistance extracted by an independent Van der Pauw measurements, for example, as disclosed in "Modern GaAs Processing Methods", by Ralph Williams, Artech House 1990. Even though the /experiment may be conducted using HEMT devices with a different material or epi stack, the experiment illustrates the validation of a semi-physical model form for Region 1 resistance. Also the terms RECsg and Lg may be assumed to be roughly constant for all of the Dsg test samples.

[0096] In the final part of the PM^2 experiment, the full form of the semi-physical source resistance model is validated. Based on the full bias dependent measurement of the part 1, the complete semi-physical model expression source resistance as a function of gate and drain bias can be represented in the equations below:

$$R_S \quad [\Omega] \quad = (R_{SundepCap} + R_{SAccess} + R_{SBoundary}) / W_g$$

$$= R_{cont}/RF_{rconF} +$$

$$R_{S\,undepCap} \quad [\Omega*\mu m] \quad R_{SH}[D_{sg} - (REC_{sg}+L_g/2)]$$

$$= R_{SdepRec}^{ON} * MR_s*\tanh\{[KC_{fK} * (V_{gs} - VC_{fOn}+V_{ds}*MC_{fL})] + 1 \} / 2 * \{ V_{gs} / 2 *[1-\tanh(KR_{sK} (V_{gs} - VR_{sOn}))]\}* \{ \tanh [KR_{sSat} (V_{ds} - VR_{sKnee})] + 1 \} / 2 + R_{SundepRec} *$$

$$R_{SAccess} \quad [\Omega*\mu m] \quad \{ \tanh[KR_{sK} (V_{gs}-VR_{sOn})] + 1\} / 2$$

$$= R_{SdepRec}^{ON} * MR_s * \tanh \{[KR_{sK}*V_{gs} + KR_{sL}*V_{ds} + VR_{sOff}] + 1 \} / 2 * \{(1+V_{ds}MR_{sL})*MR_{sK}*[1 \tanh(KR_{sSat}(V_{ds}-VR_{sKnee}))]/ [2*(1 + [V_{gs}/((1$$

$$R_{SBoundary} \quad [\Omega*\mu m] \quad + V_{ds}MR_{sL})*MR_{sK})]^{\gamma Rs})^{(1/\gamma Rs)}] \}$$

[0097] The simulated result for the sample fabricated in part 1 of the PM^2 experiments is shown in FIG. 10A. Comparing FIG. 10A with FIG. 22 indicates that the semi-physical model adequately replicates the measured results. The result of the experiment is shown below in FIG. 10B. As expected the bias dependent source resistance of the thin "cap" sample has the same form, only offset higher by an amount that corresponds to the change in Rsh in Region 1 of the source access.

S-PARAMETER MICROSCOPY

[0098] The S-parameter microscopy (SPM) method utilizes bias dependent S-parameter measurements as a form of microscopy to provide qualitative analysis of the internal charge and electrical field structure of the semiconductor device heretofore unknown. Pseudo images are gathered in the form of S-parameter measurements extracted as small signal models to form charge control maps. Although finite element device simulations have heretofore been used to calculate the internal charge/electric field of semiconductor devices, such methods are known to be relatively inaccurate. S-parameter microscopy provides a relatively accurate method for determining the internal charge and electric field within a semiconductor device. With accurate modeling of the internal charge and electric field, all of the external electrical characteristics of the semiconductor devices can be relatively accurately modeled including its high frequency performance. Thus, the system is suitable for making device technology models that enable high frequency MMIC yield analysis forecasting and design for manufacturing analysis.

[0099] S-parameter microscopy is similar to other microscopy techniques in that SPM utilizes measurements of energy reflected to and from a sample to derive information. More particularly, SPM is based on transmitted and reflective microwave and millimeter wave electromagnetic power or S-parameters. As such, S-parameter microscopy is analogous to the combined operation of scanning and transmission electron microscopes (SEM and TEM). Scattered RF energy is analogous to the reflection and transmission of the electron beams in the SEM and TEMs. However, instead of using electron detectors as in the SEM and TEMs, reflectometers in a network analyzer are used in S-parameter microscopy to measure a signal. S-parameter

microscopy is similar to other microscopy techniques in that both utilize; measurement of scattering phenomenon as data; include mechanisms to focus measurements for better resolution; and include mechanisms to contrast portions of the measurement to discriminate detail as shown in Table 3 below:

Table 3

General Microscopes	S-Parameter Microscope
Measure of ***scattered energy***	Measures ***S-Parameters***
Mechanism for ***"focus"***	Focuses by ***extraction of Unique equivalent circuit models***
Mechanism for ***"contrast"***	Contrasts by using ***bias dependence*** to finely discriminate the nature and location of charge/electric fields

[0100] RESULT: Detailed "images" of device's internal charge and electric field structure.

[0101] Images as discussed herein, in connection with S-parameter microscopy, do not relate to real images, but are used provide insight and qualitative detail regarding the internal operation of a device. More specifically, S-parameter microscopy does not provide visual images as in the case of traditional forms of microscopy. Rather, S-parameter microscopy images are more like maps which are computed and based on a non-intuitive set of measurements.

[0102] FIG. 11 illustrates a conceptual representation of an S-parameter microscope, generally identified with the reference numeral 20. The S-parameter microscope 20 is analogous to a microscope which combines the principles of SEM and TEM. Whereas SEM measures reflections and TEM measures transmissions, the 2-port S-parameter microscope 20 measures both reflective and transmitted power. As a result, data derived from the 2-port S-parameter microscope contains information about the intrinsic and extrinsic charge structure of a device. More particularly, as in known in the art, SEM provides relatively detailed images of the surface of a sample through reflected electrons while TEM provides images of the internal structure through

transmitted electrons. The reflective signals are used to form the external details of a sample while transmitted electrons provide information about the interior structure of a device. In accordance with an important aspect of the invention, S-parameter microscopy utilizes a process of measuring reflective and transmitted signals to provide similar "images" of the charge structure of a semiconductor device. As used herein the internal and external electrical structure of a semiconductor device are commonly referred to as intrinsic device region and 22 and extrinsic parasitic access region 24 as shown in FIG. 12. Also contributing to the external electrical structure of the device are parasitic components associated with its electrodes and interconnects, which are not shown. These are the so-called device "layout parasitics".

[0103] Referring to FIG. 11, the ports 26 and 28 are emulated by S-parameter measurements. The S-parameter measurements for a specific semiconductor device, generally identified with the reference number 30, are processed to provide charge control maps, shown within the circle 32, analogous to images in other microscopy techniques. These charge control maps 32, as will be discussed in more detail below, are expressed in the form of equivalent circuit models. As shown in FIG. 13, linear circuit elements are used in the models to represent the magnitude and state of charge/electric fields inside the semiconductor device 30 or its so-called internal electrical structure. The position of the circuit elements within the model topology is roughly approximate the physical location within the device structure, hence the charge control map represents a diagram of the device's internal electrical structure.

[0104] The interpretation of the exact location of measured charge/electric fields within the semiconductor device is known to be ambiguous since an equivalent circuit model, for example, as illustrated in FIG. 14 with discrete linear elements, is used to represent the distributed structure of the charge/electric fields in the actual device. Although there is no exact method for distinguishing the physical boundaries between measured quantities, bias dependence is used to clarify how the S-parameters should be discriminated, separated and contrasted. In particular, changing bias conditions is known to change the magnitude and shift boundaries between the charge and electric fields within the device. The changes are normally predictable and qualitatively well known in most technologies. As such, the charge control maps can readily be used as

maps illustrating the characterization of physical changes in magnitude, location and separation of electric charge and electric fields.

[0105] Analogous to other forms of microscopy, the S-parameter microscope 20 in accordance with the present invention also emulates a lens, identified with the reference numeral 40 (FIG. 11). The lens 40 is simulated by a method for the extraction of a unique equivalent circuit model that also accurately simulates the measured S-parameter. More particularly, parameter extraction methods for equivalent circuit models that simulate S-parameters are relatively well known. However, when the only goal is accurately fitting measured S-parameters, an infinite number of solutions exist for possible equivalent circuit parameter values. Thus, in accordance with an important aspect of the present invention, only a single unique solution is extracted which accurately describes the physical charge control map of the device. This method for unique extraction of equivalent circuit model parameters acts as a lens to focus the charge control map solution. As discussed and illustrated herein, the lens 40 is subsequently simulated by a filter that is based on an apparent layout parasitic embedding model. As discussed below, the layout parasitic embedding model consists of linear elements which simulate the effect of the device's electrodes and interconnects upon its external electrical characteristics. A Pi FET embedding model 42, is described below. This model effectively acts as a filter to remove the electrical structure of the extrinsic parasitic access contribution to the preliminary charge control map solution. The resultant filtered charge control map solution represents a clearer "image" which shows only the electrical structure of the intrinsic device. This enhanced imaging is needed in order to achieve as accurate a view of the internal electric charge/field as possible. Unlike conventional extraction techniques as illustrated in FIG. 16, which can only extract non-unique equivalent circuit models and not the unique charge control map, the S-parameter microscope 20 in accordance with the present invention is able to relatively accurately model the internal electric charge/field structure within a semiconductor device.

[0106] An exemplary application of the S-parameter microscope is illustrated in detail below. In this example, an exemplary GaAs HEMT device with four gate fingers and 200μm total gate periphery formed in a Pi-FET layout as generally illustrated in FIG. 17 and identified with the reference numeral 43, is used. The GaAs HEMT 43 is

adapted to be embedded in a 100-μm pitch coplanar test structure to facilitate on- wafer S-parameter measurement.

[0107] Initially, as illustrated in FIGS. 18 and 19, the I-V characteristics for the device are measured. In particular, the drain source current Ids is plotted as a function of drain-to-source voltage Vds at various gate voltages Vgs as shown in FIG. 18. FIG. 19 illustrates the drain-to-source current Ids as a function of gate voltage Vgs and transconductance Gm (i.e. the derivative of Ids with respect to Vgs) at different drain voltages Vds. These I-V characteristics are typical of HEMT devices, which are one type of three-terminal semiconductor device technology.

[0108] Table 4 shows the bias conditions in which S-parameters were measured. The S-parameters were measured from 0.05 to 40 GHz at each bias condition. FIG. 20 illustrates a Smith chart illustrating the measured S-parameters S11, S12 and S22 for frequencies from 0.05 to 40.0 GHz. FIG. 21 is a graphical illustration of magnitude as a function of angles for the measured S-parameter S21 for frequencies from 0.05 to 40.0 GHz.

TABLE 4
Measured S-parameter Bias Conditions

Biases / **Vgs**	**Vds = 0 V**	**Vds = 0.5 V**	**Vds = 1.0 V**	**Vds = 2.0 V**	**Vds = 4.0 V**	**Vds = 5.0 V**
-1.6 V	Yes	Yes	Yes	Yes	Yes	Yes
-1.4 V	Yes	Yes	Yes	Yes	Yes	Yes
-1.2 V	Yes	Yes	Yes	Yes	Yes	Yes
-1 V	Yes	Yes	Yes	Yes	Yes	Yes
-0.8 V	Yes	Yes	Yes	Yes	Yes	Yes
-0.6 V	Yes	Yes	Yes	Yes	Yes	Yes
-0.4 V	Yes	Yes	Yes	Yes	Yes	Yes
-0.2 V	Yes	Yes	Yes	Yes	Yes	Yes
0 V	Yes	Yes	Yes	Yes	Yes	Yes
0.2 V	Yes	Yes	Yes	Yes	Yes	Yes
0.4 V	Yes	Yes	Yes	Yes	Yes	Yes
0.6 V	Yes	Yes	Yes	Yes	Yes	Yes

[0109] Using the small signal model illustrated in FIG.14, the extracted small signal equivalent circuit values are obtained as illustrated in Table 5 for each S-parameter at each bias condition, using the extraction method discussed below.

Table 5

Bias-dependent Small-signal Equivalent Circuit Models

Vd [V]	Vg [V]	Rg+Ri [W]	Rs [W]	Rd [W]	Lg [nH]	Ls [nH]	Ld [nH]	Cgs [pF]	Cdg [pF]	Cds [pF]	Gm [mS]	Rds [W]	Tau [pS]	Rgs [W]	Rgd [W]
0	-2	4.32849	0.51256	4.2	0.01972	0.00001	0.02650	0.04154	0.04154	0.04324	0	10000000	0	904000000	904000000
0	-1.6	4.11231	0.52	4	0.028	0	0.0245	0.045	0.045	0.045	0	10000000	0	87000	87000
0	-1.4	3.01231	0.55	3.53898	0.02754	0.00001	0.02343	0.05012	0.05012	0.046	0	1000000	0	70000	70000
0	-1.2	3.97956	0.58579	3.92313	0.02740	0.00001	0.02455	0.05497	0.05497	0.04674	0	3532.954	0	59895.6	59895.6
0	-1	3.67822	0.58	3.7	0.02634	0.00123	0.0253	0.06322	0.06322	0.047	0	200	0	60000	60000
0	-0.8	3.39996	0.58	3.67134	0.02622	0.00347	0.02597	0.08009	0.08009	0.04883	0	51.8679	0	60000	60000
0	-0.6	3.33401	0.58579	3.50319	0.02764	0.00353	0.02398	0.0923	0.0923	0.15973	0	7.84388	0	970000000	970000000
0	-0.4	3.31632	1.76777	3.3	0.02324	0.00356	0.03387	0.10025	0.10025	0.18057	0	6.65812	0	65565.93	65565.93
0	-0.2	3.09963	1.76777	3.3	0.02421	0.00347	0.03443	0.10446	0.10446	0.42106	0	4.75859	0	58682.78	58682.78
0	0	3.16448	1.41421	3.5	0.01566	0.00334	0.03144	0.10768	0.10768	0.45837	0	3.49009	0	55000	55000
0	0.2	2.45244	1.28033	3.30807	0.02664	0.00384	0.02818	0.11001	0.11001	1.67455	0	1.40002	0	16926.72	16926.72
0	0.6	2.48828	1.41421	2.61956	0.02664	0.00352	0.02845	0.12479	0.12479	2.02904	0	1.25101	0	3811.933	3811.933
0	0.755	4.31968	1.5	2.3	0.01881	0.00320	0.03089	0.14170	0.14170	2	0	2.94325	0	478.3791	478.3791
0.5	-1.6	4.80961	0.5	4	0.03374	0.0	0.01699	0.04725	0.03892	0.04621	0.223	1.02E+08	0.12	100403	8.10E+07
0.5	-1.4	**4.24223**	0.5	3.53898	0.02817	0.0	0.02476	0.05172	0.03907	0.04440	**0.5**	**10000000**			
0.5	-1.2	3.91986	0.5	3.92313	0.02913	0.00030	0.02260	0.05921	0.03981	0.04616	0.732	1.08E+08	0.67	24714.05	9.23E+07
0.5	-1	3.25620	0.85355	3.7	0.02881	0.00354	0.02758	0.07264	0.03983	0.04586	5.672	7.00E+02	0.24	9.90E+07	98010
0.5	-0.8	3.22405	0.7	3.67134	0.02841	0.00319	0.02461	0.09074	0.04253	0.04625	28.00	254.802	0.26	69641.32	69641.32
0.5	-0.6	2.78789	0.6	3.50319	0.02953	0.00337	0.02583	0.10155	0.04589	0.04748	73.80	84.25923	0.16	16066.22	6.36E+07
0.5	-0.4	1.71421	0.6	3.3	0.03058	0.00343	0.02529	0.08533	0.05957	0.0669	107.5	38.90041	0.00	8.77E+07	77782.14
0.5	-0.2	**0.14250**	**3.3**	**3.3**	0.01976	3.78E-09	0.02305	0.14987	0.05706	0.35247	116	9.43176	0.03	18440.35	9.70E+07
0.5	0	2.35912	3.4	3.4	0.02067	0.00373	0.01532	0.16889	0.09085	0.5	108	7	150.	1.00E+08	1.00E+08
0.5	0.2	1.38026	3.5	3.30807	0.01797	0.00563	0.02082	0.21366	0.04018	1.4	100	1.45897	447.	9915.727	1.00E+08
0.5	0.4	1.56731	3.5	3.00269	0.02537	0.00556	0.02100	**0.115**	**0.115**	2	85	1.2	156.	8630.088	9.90E+07
0.5	0.6	1.54964	3.6	2.61956	0.03453	0.00356	0.02748	0.219	0.00152	2.1	75	1.4	0.06	28918.35	9.90E+07
1	-1.6	0.04221	0.5	3.9	0.03766	0.00001	0.01	0.04706	0.03607	0.04717	0.038	1.03E+08	735	10980.53	1.02E+08
1	-1.4	5.37668	0.5	3.53120	0.04292	0.00070	0.01	0.04880	0.03632	0.04857	0.086	1.23E+08	0.14	71680.16	9.70E+07
1	-1.2	3.73022	0.6	4.38390	0.02639	0.0	0.03059	0.06252	0.03581	0.04551	1.391	1.03E+08	0.81	42870.63	1.00E+08
1	-1	2.83050	2.6	3.7	0.03139	0.00013	0.02741	0.07956	0.03434	0.04721	8.764	6.96E+07	0.24	9.80E+07	97029.9
1	-0.8	3.38450	0.6	3.35829	0.02891	0.00373	0.02546	0.10424	0.03365	0.04472	37.04	266.1964	0.50	54006.62	136132.8

1	-0.6	3.00864	0.5	2.68486	0.02976	0.00429	0.02666	0.12806	0.02974	0.04391	80.28	132.6002	0.39	68255.46	136132.8
1	-0.4	2.20164	1	5.24976	0.03200	0.00355	0.02466	0.13702	0.02568	0.05399	104.4	113.1406	0.15	139239.2	153397.8
1	-0.2	1.77701	1.4	6.13975	0.03218	0.00296	0.02378	0.14376	0.02312	0.06141	116	94.51954	0.08	5067.04	153397.8
1	0	2.04598	1.2	3.76638	0.03204	0.00341	0.02636	0.14735	0.02295	0.06126	108	116.7009	0.12	82594.56	153397.8
1	0.2	2.25956	1.1	0.67552	0.03031	0.00405	0.02972	0.15401	0.02543	0.06518	100	97.92344	0.26	62352.54	159626.4
1	0.4	2.11654	1.4	1.20729	0.03023	0.00451	0.02767	0.15538	0.03258	0.09048	82.93	46.7057	0.22	62140.25	143076.9
1	0.6	2.68064	1.06066	0.53210	0.02779	0.00522	0.02902	0.15025	0.04746	0.10476	59.07	29.71128	0.31	32295.59	9.41E+07
2	-1.6	4.21832	0.36612	3.64439	0.02169	0.00007	0.02715	0.04902	0.03373	0.04284	0.018	3.74E+07	4.00	86865.89	117257.9
2	-1.4	4.16045	0.35355	3.78284	0.03206	0.0	0.00986	0.05184	0.03363	0.04633	0.321	2.26E+08	1.55	7.62E+07	7.62E+07
2	-1.2		0.4	3.3											
2	-1	3.97092	0.4	2.95737	0.01991	0.00355	0.02582	0.08850	0.03172	0.04346	14.66	752.2115	0.94	11969.85	143076.9
2	-0.8	3.43921	0.58579	3.03263	0.02177	0.00369	0.02686	0.10341	0.03367	0.04403	36.71	267.6627	0.52	9.90E+07	101000
2	-0.6	3.14409	0.85355	2.82957	0.02363	0.00351	0.02706	0.15517	0.02427	0.04545	86.93	150.9714	0.56	66897.18	148886.4
2	-0.4	2.61645	1.06066	4.45931	0.02464	0.00350	0.02666	0.16323	0.02155	0.05049	109.7	138.1298	0.34	138869	138869
2	-0.2	2.16237	1	5.63054	0.02558	0.00343	0.02524	0.15694	0.01990	0.05282	115.9	144.5568	0.24	29720.56	154931.8
2	5.40E-	2.31075	0.9	5	0.02351	0.00358	0.02701	0.15357	0.01906	0.04803	108.1	157.9708	0.36	42443.77	143076.9
2	0	2.09877	0.85355	4.76720	0.02557	0.00359	0.02535	0.15291	0.01879	0.05078	109.2	155.8182	0.27	19029.68	125716.3
2	0.2	2.64301	0.85355	3.23486	0.0244	0.00356	0.02808	0.15727	0.01802	0.04871	96.42	163.3582	0.27	81117.65	1.10E+08
2	0.4	3.03424	0.85355	1.80413	0.02341	0.00356	0.02901	0.16401	0.01776	0.04788	79.14	171.8245	0.33	95099.01	1.05E+08
2	0.6	3.45639	1	0.61175	0.02245	0.00351	0.02800	0.17494	0.01767	0.04798	63.09	179.6613	0.48	47169.75	1.27E+08
4	-1.6	1	0.6	3.6	0.03900	0.00007	0.01	0.04765	0.03174	0.04984	0.111	8.95E+07	5.46	15181.61	9.90E+07
4	-1.4	4.71381	0.5	3.43796	0.02063	0.00014	0.02710	0.05937	0.03122	0.04303	1.410	7171.182	1.58	8.02E+07	1.24E+08
4	-1.2	4.42193	1.3	3.2	0.02717	0.00002	0.00124	0.07691	0.02927	0.05239	7.582	1.03E+08	1.52	75390.74	9.51E+07
4	-1	4.28211	1.6	3.1306	0.02220	0.00226	0.02517	0.11961	0.02672	0.04456	31.09	417.6118	1.08	72214.74	102010
4	-0.8	3.92452	1.5	3.05507	0.02333	0.00280	0.02668	0.16912	0.02270	0.04603	68.77	204.0465	0.84	35767.7	147412.3
4	-0.6	3.45589	1.3	3.81853	0.02435	0.00303	0.02526	0.19074	0.02048	0.04833	93.20	171.7183	0.71	32817.08	148886.4
4	-0.4	3.15713	1.4	5.52029	0.0254	0.00245	0.02235	0.19523	0.01899	0.05190	109.7	167.8084	0.57	8.77E+07	150375.2
4	-0.2	3.03221	1.1	3.87285	0.02483	0.00311	0.02631	0.18804	0.01819	0.04922	108.9	184.4907	0.56	31725.31	148886.4
4	0	2.78474	1	2.7	0.02499	0.00425	0.02735	0.17509	0.01774	0.04685	95.97	207.0277	0.59	25879.99	150375.2
4	0.2	3.24209	0.9	1.48994	0.02404	0.00381	0.02868	0.17879	0.01685	0.04634	83.82	212.1484	0.55	8.86E+07	153397.8
4	0.4	3.99720	0.8	1.2	0.02037	0.00414	0.02095	0.20669	0.01786	0.06562	83.82	151.6078	0.55	95099.01	105101
4	0.6	3.85544	1	1.12128	0.02333	0.00299	0.02312	0.19731	0.01611	0.04746	52.91	231.8809	0.75	16152.41	136132.8
5	-1.6	3.83032	0.4	3.6	0.02626	0.01559	0.03312	0.04802	0.03134	0.03869	0	4592.258	0	1.00E+09	106152
5	-1.4	4.28848	1.4	3.4	0.02174	0.0	0.02839	0.06338	0.03006	0.04302	2.804	8.62E+07	1.60	83451.39	119614.8
5	-1.2	4.21790	2	3.3	0.01536	0.00341	0.02351	0.09669	0.03007	0.04316	0	386.3951	0	19446.95	109368.5

5	-1	4.47178	1.8	2.87325	0.02239	0.00199	0.02521	0.14703	0.02426	0.04505	46.24	293.0981	1.08	7.25E+07	137494.1
5	-0.8	3.78294	1.5	3.46025	0.02367	0.00317	0.02437	0.18748	0.02118	0.04735	77.13	195.8661	0.88	9.61E+07	89446.16
5	-0.6	3.43996	1.5	5.26075	0.02469	0.00289	0.02161	0.20516	0.01940	0.05136	97.94	177.1967	0.70	8.69E+07	140364.4
5	-0.4	3.24864	1.1	3.41057	0.02427	0.00372	0.02454	0.20480	0.01867	0.04869	103.1	189.0745	0.74	7.78E+07	120940.4
5	-0.2	3.36600	1	2.43302	0.02418	0.00316	0.02679	0.20094	0.01771	0.04718	102.8	198.7121	0.76	9.04E+07	67628.66
5	0	3.66823	1	1	0.02364	0.00238	0.03020	0.20166	0.01647	0.04563	101	102.8015	0.76	1.13E+08	27192.43
5	0.2	3.60190	1.1	0.60143	0.02392	0.00260	0.02939	0.20083	0.01544	0.04509	77.64	183.0196	0.79	1.08E+08	14811.42
5	0.4	4.21933	1.2	0.6	0.02300	0.00249	0.02825	0.21695	0.01552	0.05731	65	133.1078	0.81	1.00E+09	8890.916
5	0.6	3.80536	1.2	0.5	0.02404	0.00292	0.02127	0.21078	0.01532	0.04376	44	157.4825	1.20		

[0110] The values in Table 5 represent solutions that are close to the charge control map and represent physically significant solutions of the FET's electrical structure. However, the values represented in Table 5 contain the influence of external layout parasitics which are subtracted using a model for the embedding parasitics to obtain the most accurate charge control mapping to the intrinsic device characteristic. In particular, an embedding model is applied to filter the extracted equivalent circuit model values to obtain values more representative of the intrinsic device. In particular, in the exemplary embodiment, a PiFET embedding parasitic model is used to subtract capacitive contributions due to interelectrode and off-mesa layout parasitic influences. This filter essentially subtracts known quantities formed from the parameters Cgs, Cgd and Cds depending on the device layout involved. In this example, embedding of the inductive parameters is not necessary because these quantities are extrinsic and do not contribute to the charge control map of the intrinsic device.

[0111] As discussed above, the lens with filter is used to generate unique charge control maps. In particular, FIGS. 22-25 illustrate the bias dependent charge control maps for the parameters RS, RD, RI, CGS and CGD as a function of bias. More particularly, FIG. 22 illustrates a charge control map of the charge and electric field distribution in the on-mesa source access region illustrated by the source resistance R_s as a function of bias. FIG. 23 illustrates a charge control map of the charge and electric field distribution in the on-mesa drain access region illustrated by the drain resistance R_d as a function of bias. FIG. 24 illustrates a charge control map for a non-quasistatic majority carrier transport illustrated by the intrinsic device charging resistance R_i as a function of gate bias for different drain bias points. FIG. 25 illustrates a charge control map for gate modulated charge and distribution under the gate shown with the gate capacitance CGS and CGD as a function of bias.

FILTER

[0112] As mentioned above, the S-parameter microscope 20 utilizes a filter to provide a clearer charge control map for modeling the internal electric charge/field of a semiconductor device. Although the filter is illustrated in connection with the PiFET with multiple gate fingers, as illustrated in FIGS. 26 and 27, the principles of the invention are applicable to other semiconductor devices.

[0113] As illustrated in FIG. 26, PiFETs are devices in which the gate fingers and the edge of the active region resemble the greek letter π, as illustrated. Such PiFET layouts facilitate construction of multi fingered large periphery device cells, for example, as illustrated in FIG 27. In accordance with an important aspect of the invention, the multi-finger semiconductor device is modeled as a combination of single finger device cells. Each single finger device cell is represented by a hierarchy of four models, which, in turn, are assembled together using models for interconnects to represent an arbitrary multi-fingered device cell, illustrated in FIG. 28. The four models are as follows: off mesa or boundary parasitic model; interelectrode parasitic model; on-mesa parasitic model and intrinsic model.

[0114] The off-mesa parasitic model is illustrated in FIG. 29. This model represents the parasitics that exist outside the active FET region for each gate finger. In this model, the fringing capacitance of each gate finger off the active device region as well as the off-mesa gate finger resistance is modeled.

[0115] The interelectrode parasitic model and corresponding equivalent circuit are illustrated in FIGS. 30-32. This model represents parasitics between the metal electrodes along each gate finger. The following fringing capacitance parasitics are modeled for the gate-to-source air bridge; drain-to-source air bridge; gate-to-source ohmic; gate-to-drain ohmic and source-to-drain ohmic as generally illustrated in FIG. 31.

[0116] The on-mesa parasitic model and corresponding equivalent circuit are illustrated in FIGS. 33 and 34. This model represents that parasitics around the active FET region along each gate finger including various capacitance fringing parasitics and

resistive parasitics. In particular, the gate-to-source side recess; gate-drain-side recess; gate-source access charge/doped cap; and gate-drain access charge/doped cap capacitance fringing parasitics are modeled. In addition, the gate metallization and ohmic contact resistive parasitics are modeled.

[0117] The intrinsic model and corresponding equivalent circuit are illustrated in FIGS. 35 and 36. The intrinsic model represents the physics that predominately determine the FET performance. In particular, the DC and current voltage response can be determined by physics based analytical equations for magnitude and location of intrinsic charge which are generally know in the art, for example, as disclosed in "Nonlinear Charge Control in AlGaAs/GaAs Modulation-Doped FETs", by Hughes, et al., IEEE Trans. Electron Devices, Vol. Ed-34, No. 8, August 1987. The small signal model performance is modeled by taking a derivative of the appropriate charge or current control equations to derive various terms such as RI, RJ, RDS, RGS, RGD, GM, TAU, CGS, CDS and CGD. Such control equations are generally known in the art and disclosed in detail in the Hughes et al reference mentioned above, hereby incorporated by reference. The noise performance may be modeled by current or voltage perturbation analysis "Noise Characteristics of Gallium Arsenride Field-Effect Transistors" by H. Statz, et al, IEEE-Trans. Electron Devices, vol. ED-21, No. 9, September 1974 and "Gate Noise in Field Effect Transistors at Moderately High Frequencies" by A. Van Der Ziel, Proc. IEEE, vol 51, March 1963.

[0118] An example of a parasitic model for use with the S-parameter microscopy discussed above is illustrated in FIGS. 37-44. Although a specific embodiment of a semiconductor device is illustrated and described, the principles of the present invention are applicable to various semiconductor devices. Referring to FIG. 37, a Pi-FET is illustrated. As shown, the PiFET has four gate fingers. The four fingered Pi-FET is modeled in FIG. 37. In particular, FIG 37 illustrates an equivalent circuit model for Pi-FET illustrated in FIG. 36 as implemented by a known CAD program, for example, LIBRA 6.1 as manufactured by Agilent Technologies. As shown, the equivalent circuit models does not illustrate all of the equivalent circuit elements or network connections involved with implementing the parasitic embedding models, but rather demonstrates

a finished product. FIG. 37 is displayed in symbol view in order demonstrate resemblance to FIG. 9. The actual technical information regarding the construction of the network and its equivalent circuit elements are normally provided in schematic view.

[0119] FIGS. 38-44 demonstrate the application of the parasitic model for use with the S-parameter microscopy. An important aspect of the parasitic modeling relates to modeling of multi-gate fingered devices as single gate finger devices. As used herein, a single unit device cell refers to a device associated with a single gate finger. For example, a four fingered Pi-FET as illustrated in FIG. 37 is modeled as four unit device cells.

[0120] Initially, the four finger Pi-FET illustrated in FIG. 37, is modeled as a single finger unit device cell 100 with an intrinsic model 102, as shown in FIGS. 38 and 39. In particular, the Pi-FET intrinsic FET model 104 is substituted for the block 102 defining a first level of embedding. As shown in FIG. 39, the parameter values for the Pi-FET intrinsic model are added together with the parameter values for the single fingered unit device cell intrinsic model. The intrinsic device model 104 may be developed by S-parameter microscopy as discussed above. Next, as illustrated in FIG. 40, the interconnect layout parasitic elements are added to the equivalent model by simply adding the model terms to the value of the appropriate circuit element to form a single unit device cell defining a second level of embedding. Once the single unit device cell is formulated, this device is used to construct models for multi-fingered devices. In this case, a Pi-FET with four gate fingers is modeled as four single finger device unit cells as shown in FIG. 41. Subsequently, the off-mesa layout parasitic elements are connected to the multi-fingered layout, defining a third level of embedding as illustrated in FIG. 42. These off-mesa layout parasitic elements, generally identified with the reference numerals 108 and 110, are implemented as new circuit elements connected at key outer nodes of the equivalent circuit structure. Subsequently, a fourth level of embedding is implemented as generally illustrated in FIG. 46. In particular, an inductor model is connected to the sources of each of the various unit device cells to represent the metallic bridge interconnection, as generally shown in FIG. 43. Lastly,

as illustrated in FIG. 45, a fifth level of embedding is implemented in which the feed electrodes model 114 and 116 are modeled as lumped linear elements (i.e. capacitors inductors) as well as the distributive elements (i.e. microstrip lines and junctions) to form the gate feed and drain connections illustrated in FIG. 44. As shown, the distributive elements are distributed models for microstrip elements as implemented in LIBRA 6.1.

EXTRACTION METHOD FOR UNIQUE DETERMINATION OF FET EQUIVALENT CIRCUIT MODELS

[0121] The method for determining FET equivalent circuit parameters as discussed above is illustrated in FIGS. 45-50. This method is based on an equivalent circuit model, such as the common source FET equivalent circuit model illustrated in FIG. 14. Referring to FIG. 45, a model is initially generated in step 122. The model illustrated in FIG. 14 is used as a small signal model for the FET. In accordance with an important aspect of the algorithm, the equivalent circuit parameters are based upon measured FET S-parameters. Measurement of S-parameters of semiconductor devices is well known in the art. FIG. 48 is a Smith chart illustrating exemplary measured S-parameters S11, S12 and S22 for frequencies between 0.05 to 40 GHz. FIG. 48 represents a magnitude angle chart for the measured S-parameter S21 from frequencies from 0.05 to 40 GHz. After the S-parameters are measured, as set forth in step 124 (FIG. 45), it is ascertained whether the measurements are suitable in step 126. This is either done by manually inspecting the test result for anomalies, or by algorithms to validate the test set. If the measurements are suitable, the S-parameter measurements are stored in step 128.

[0122] A space of trial starting feedback impedance point values, for example, as illustrated in Table 6 is chosen. Then, a direct model extraction algorithm, known as the Minasian algorithm, is used to generate preliminary values for the equivalent circuit model parameters, for each value of starting feedback impedance. Such extraction algorithms are well known in the art, for example, as disclosed "Broadband Determination of the FET Small Equivalent Small Signal Circuit" by M. Berroth, et al.,

IEEE - MTT, Vol. 38, No. 7, July 1990. Model parameter values are determined for each of the starting impedance point values illustrated in Table 6. In particular, referring to FIG. 45A, each impedance point in Table 6 is processed by the blocks 130, 132, etc. to develop model parameter values for each of the impedance point in order to develop an error metric, which, in turn, is used to develop a unique small signal device model, as will be discussed below. The processing in each of the blocks 130, 132 is similar. Thus, only a single block 130 will be discussed for an exemplary impedance point illustrated in Table 6. In this example, the feedback impedance point 17 which correlates to a source resistance R_s ohm of 1.7Ω and a source inductance L_s of 0.0045pH is used.

TABLE 6
Trial Starting Feedback, Impedance Space Point Values

Impedance Point	Resistance (Rs)	Inductance (Ls)
1	0.1 Ω	0.0045 pH
2	0.2 Ω	0.0045 pH
3	0.3 Ω	0.0045 pH
4	0.4 Ω	0.0045 pH
5	0.5 Ω	0.0045 pH
6	0.6 Ω	0.0045 pH
7	0.7 Ω	0.0045 pH
8	0.8 Ω	0.0045 pH
9	0.9 Ω	0.0045 pH
10	1.0 Ω	0.0045 pH
11	1.1 Ω	0.0045 pH
12	1.2 Ω	0.0045 pH
13	1.3 Ω	0.0045 pH
14	1.4 Ω	0.0045 pH
15	1.5 Ω	0.0045 pH
16	1.6 Ω	0.0045 pH
17	1.7 Ω	0.0045 pH
18	1.8 Ω	0.0045 pH
19	1.9 Ω	0.0045 pH

20	2.0 Ω	0.0045 pH
21	2.1 Ω	0.0045 pH
22	2.2 Ω	0.0045 pH
23	2.3 Ω	0.0045 pH
24	2.4 Ω	0.0045 pH
25	2.5 Ω	0.0045 pH
26	2.6 Ω	0.0045 pH
27	2.7 Ω	0.0045 pH
28	2.8 Ω	0.0045 pH
29	2.9 Ω	0.0045 pH
30	3.0 Ω	0.0045 pH

[0123] For the selected value, $R_s = 1.7$ ohms, initial intrinsic equivalent circuit parameters and initial parasitic equivalent circuit parameter are determined, for example, by the Minasian algorithm discussed above and illustrated in Tables 7 and 8 as set forth in steps 134 and 136. In step 138 the simulated circuit parameters are compared with the measured S-parameters, for example, as illustrated in FIGS. 48A and 48B. Each of the processing blocks 130 and 132 etc. goes through a fixed number of complete cycles, in this example, six complete cycles. As such, the system determines in step 140 whether the six cycles are complete.

TABLE 7
Initial "Intrinsic" Equivalent Circuit Parameters

Intrinsic Equivalent Circuit Parameter	Initial Solution
Cgs	0.23595 pF
Rgs	91826 Ω
Cgd	0.0177 pF
Rgd	100000 Ω
Cds	0.04045 pF
Rds	142.66 Ω
Gm	142.1025 mS
Tau	0.1 pS

TABLE 8
Initial "Parasitic" Equivalent Circuit Parameters

Intrinsic Equivalent Circuit Parameter	Initial Solution
Rg	3.0 Ω
Lg	0.014 nH
Rs	1.7 Ω
Ls	0.0045 nH
Rd	2.5 Ω
Ld	0.024 nH

[0124] Each cycle of the processing block 130 consists of a direct extraction followed by an optimization with a fixed number of optimization iterations, for example 60. By fixing the number of extraction-optimization cycles along with the number of optimization iterations, a fixed "distance" or calculation time which the model solution must be derived is defined. As such, the algorithm implements a convergence speed requirement of the global error metric by setting up an environment where each trial model solution competes against each other by achieving the lowest fitting error over a fixed calculation time thus causing a "race" criteria to be implemented, where "convergence speed" is implicitly calculated for each processing block 130, 132 etc.

[0125] After the system determines whether the racing is done in step 140, the system proceeds to block 142 and optimizes model parameters. Various commercial software programs are available, for example, the commercially available LIBRA 3.5 software as manufactured by HP-eesof, may be used both for circuit simulation as well as optimizing functions. The optimization is performed in accordance with the restrictions set forth in Table 9 with the addition of fixing the feedback resistance R_s to a fixed value.

TABLE 9
Environment Used for Competitive Solution Strategy, as Implemented in this Example

Implementation Parameter	
Circuit Simulator and Optimizer	Libra 3.5
Optimization Algorithm	Gradient
Optimization Error Metric	Mag and angle of S11,S21,S12,and S22 from 4 to 40 GHz
Number of Iterations	60
Number of Extraction/Optimization Cycles	6

[0126] By fixing the value for R_s this segment of the algorithm is confined to creating a trial model solution for only the trial feedback impendence point with which it started. Table 10 illustrates the optimized intrinsic equivalent parameter values using commercially available software, such as LIBRA 3.5. These values along with the optimized parasitic values, illustrated in Table 11, form the first optimized model solution for the first extraction-optimization cycle (i.e. one of six). The optimized model parameters are then fed back to the function block 134 and 136 (FIG. 45 and used for a new initial model solution. These values are compared with the measured S-parameter value as illustrated in FIGS. 49A and 49B. The system repeats this cycle for six cycles in a similar fashion as discussed above. After the six extraction-optimization cycle, the final trial model solution for the trial impendence point 17 is complete along with its final fitting error to the measured data to form the new error metric 144. In accordance with an important aspect, the extraction-optimization algorithm makes the final optimization fitting error for each point implicitly carry information about both the measured to model fitting error and the speed of convergence. It does so by the fixed optimization time constraint which sets up a competitive race between the various trial model solutions.

TABLE 10
Optimized "Intrinsic" Equivalent Circuit Parameters

Intrinsic Equivalent Circuit Parameter	Initial Solution
Cgs	0.227785 pF
Rgs	65247 Ω
Cgd	0.017016 pF
Rgd	130820 Ω
Cds	0.047521 pF
Rds	160.18 Ω
Gm	135.74 mS
Tau	0.446 pS

TABLE 11
Optimized "Parasitic" Equivalent Circuit Parameters

Intrinsic Equivalent Circuit Parameter	Initial Solution
Rg	4.715 Ω
Lg	0.02903 nH
*Rs**	*1.7 Ω*
Ls	0.002102 nH
Rd	3.2893 Ω
Ld	0.0317 nH

[0127] The implementation of the extraction optimization cycles makes the best and fastest solving solution appear as a global minima for the final fitting error in step 146 of all of the trial impedance points as generally shown in FIGS. 46 and 47. More specifically, referring to FIG. 46 the global minima solution using the new error metric is found around R_s=1.7 ohms. Tables 12 and 13 list the final model equivalent circuit parameters for this global solution, including the intrinsic and parasitic parameter as set forth in step 148 (FIG. 45B).

TABLE 12
Global Solution for "Intrinsic" Equivalent Circuit Parameters

Intrinsic Equivalent Circuit Parameter	Initial Solution
Cgs	0.227745 pF
Rgs	64242 Ω
Cgd	0.017019 pF
Rgd	133450 Ω
Cds	0.047544 pF
Rds	160.1791 Ω
Gm	135.7568 mS
Tau	0.443867 pS

TABLE 13
Global Solution "Parasitic" Equivalent Circuit Parameters

Extrinsic Equivalent Circuit Parameter	Initial Solution
Rg	4.711895 Ω
Lg	0.029314 nH
Rs	*1.7 Ω*
Ls	0.002104 nH
Rd	3.309899 Ω
Ld	0.031671 nH

[0128] In order to test the accuracy of the solution, the final model for solutions are compared with the measured S-parameter values as shown in FIGS. 50A and 50B. As shown, there is good correlation between the simulated model values and the measured S-parameters values thus verifying that the simulated model values represent a relatively accurate and unique small signal device model.

[0129] Obviously, many modifications and variations of the present invention are possible in light of the above teachings. Thus, it is to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than as specifically described above.

[0130] What is claimed and desired to be covered by a Letters Patent is as follows: